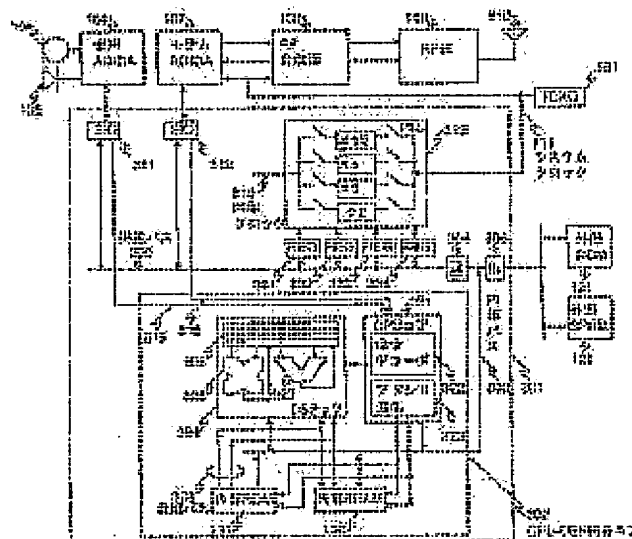


ref. 2

DIGITAL COMMUNICATION TERMINAL EQUIPMENT**Publication number:** JP11252001 (A)**Publication date:** 1999-09-17**Inventor(s):** HATANO YUJI; NAKAGAWA TETSUYA; KIUCHI ATSUSHI**Applicant(s):** HITACHI LTD**Classification:****- international:** H04B7/26; H04Q7/38; H04B7/26; H04Q7/38; (IPC1-7): H04B7/26; H04Q7/38**- European:****Application number:** JP19980050977 19980303**Priority number(s):** JP19980050977 19980303**Abstract of JP 11252001 (A)**

PROBLEM TO BE SOLVED: To reduce the size of terminal equipment and power consumption by avoiding the use of a high-speed clock signal at all the time by adopting a DSP-CPU connecting chip and adopting respectively suitable clock frequencies at the time of digital signal processing, equipment control and base station switching or at the time of soundless voices. **SOLUTION:** A DSP-CPU integrated chip 301 is used for housing a DSP core 423 and a CPU core 321 while sharing an instruction decoder 322 and for housing a clock signal generating circuit 313 together. To the DSP core 324 and the CPU core 321, an internal clock signal 113 at high speed in the case of digital signal processing to operate both the cores and at low speed in the case of following equipment control to use only the CPU core 321 is supplied from the generating circuit 313. Time dividing operation for alternately repeating this operation is adopted, the internal clock signals 113 at plural optimum frequencies are supplied, and the state of consuming no power at the time of base station switching or the like can be provided. Thus, the number of IC chips and power consumption can be reduced.



Data supplied from the esp@cenet database — Worldwide

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]A signal processing unit which performs digital signal processing of a signal transmitted and received (henceforth "DSP").

A central processing unit which performs various kinds of appliance control including communications protocol control (henceforth "CPU").

A clock signal generating circuit.

An instruction decoder for being digital communication terminal equipment provided with the above, and controlling DSP and CPU, It is constituted by single instruction decoder shared between both sides of DSP and CPU, and a clock signal generating circuit, The same clock signal is supplied to both sides of DSP and CPU, and it is characterized by being that to which only a CPU is higher than the 2nd frequency of a clock signal at the time of operation, and both sides of DSP and CPU set the 1st frequency of a clock signal at the time of operation.

[Claim 2]The digital communication terminal equipment according to claim 1 with which said DSP is characterized by said CPU being in a low-power-consumption state from CPU in response to a command of reduce power consumption during appliance control execution.

[Claim 3]A period when said CPU performs operation for which said clock signal generating circuit switches a base station under communication to other base stations,

The digital communication terminal equipment according to claim 1 being what sets clock signal frequency at the time of DSP and CPU [both] operation as the 3rd frequency higher than said 1st frequency.

[Claim 4]The digital communication terminal equipment according to claim 1 being that by which predetermined carries out renewal of period, and it sets clock signal frequency at the time of DSP and CPU [both] operation as the 4th frequency lower than said 1st frequency when a signal which transmits and receives said clock signal generating circuit is below a predetermined level.

[Claim 5]When communication with a base station is carried out by a Time Division Multiple Access, In periods other than a transceiver time slot by which said clock signal generating circuit is assigned to a self-terminal, The digital communication terminal equipment according to claim 3, wherein it sets clock signal frequency at the time of DSP and CPU [both] operation as the 5th frequency higher than said 3rd frequency and a clock signal of the 5th frequency concerned has [and] an asynchronous relation with a clock signal of the 3rd frequency.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to the digital communications terminal which transmits and receives the signal which applied between base stations to the communications system which communicates using a radio frequency band, and started the suitable terminal, especially digitized.

[0002]

[Description of the Prior Art]As an example of conventional digital communication terminal equipment, it is a catalog of U.S. AT & T Microelectronics. The terminal indicated to [BC94-006GSM "GSM Hardware Platform" (February, 1994 issue)] is shown in drawing 9. As for the terminal, DSP(Digital Signal Processor) 103 performs digital signal processing of an audio signal, CPU(Central Processing Unit) 102 performs appliance control (communications protocol control with a base station, and motion control of each part article of the inside of a terminal). CPU102 is constituted by the microprocessor (micro Processor).

[0003]Since DSP103 and CPU102 are the hardwares separated with the respectively different IC chip, It can be defined as the discrete type Two Engines, DSP103 operates with the optimal high speed clock signal, and the parallel operation of operating with the optimal low speed clock signal is possible for CPU102. In order to make this parallel operation possible, it is indicated to JP,60-502274,A and the publicly known frequency multiplying PLL (Phase Locked Loop) circuit is used as the clock signal generating circuit 112 of DSP103 built-in. The clock signal generating circuit 112 outputs the high speed clock signal 113 which carries out frequency multiplying of the system clock signal 111, and is supplied to DSP103. On the other hand, the system clock signal 111 which is a low speed clock signal is supplied to CPU102.

[0004]However, since the discrete type Two Engines is used, an instruction decoder is needed in this Prior art, for an inside by each of DSP103 and CPU102. There was a problem that the part chip size and power consumption with which an instruction decoder will be two pieces became large, and the size and power consumption of a terminal became large.

[0005]

[Problem(s) to be Solved by the Invention]While accommodating both DSP and CPU recently, IC of unified type Single Engine which made the instruction decoder of CPU substitute for the instruction decoder of DSP was developed by Hitachi, Ltd. [For example, refer to U.S. "Proceedings of The Processing Application Conference at DSP'96" the 645th page - the 652nd page (March, 1996 issue).] .

[0006]Therefore, if IC which has this integrated instruction decoder is used for a terminal, a chip size and power consumption become small and the size and power consumption of a terminal can be made small. However, since DSP is controlled by the instruction decoder of CPU in this case, On the other hand, it became clear at the time of DSP operation that the separated supply of the clock signal of supplying a high speed clock signal to DSP on the other hand was impossible, supplying a low speed clock

signal to CPU, and a high speed clock signal had to be supplied to both CPU and DSP. That is, it is impossible to make the parallel operation of low speed clock operation of CPU like [in the case of the terminal using the discrete type Two Engines] and high-speed clock operation of DSP perform to unified type Single Engine. It is the futility of electric power to use a high speed clock signal for the appliance control by CPU, and there was a problem that the reduce power consumption of a terminal was difficult.

[0007]The purpose of this invention is to provide the new digital communication terminal equipment which can solve said problem of conventional technology, and can reduce the number of IC chips, and can reduce power consumption.

[0008]

[Means for Solving the Problem]Said SUBJECT of this invention supplies the same clock signal to both sides of DSP and CPU while making an instruction decoder of CPU substitute for an instruction decoder of DSP, And solving effectively is possible, when only a CPU is higher than frequency (the 2nd frequency) of a clock signal at the time of operation and both sides of DSP and CPU set up frequency (the 1st frequency) of a clock signal at the time of operation. Operate both sides of DSP and CPU and digital signal processing is performed, Then, only a CPU operates appliance control, it is performed and it becomes possible to adopt time division operations which repeat this by turns, It is because supply of the same optimal clock signal as a case of the conventional discrete type Two Engines of supplying a high-speed clock signal at the time of digital signal processing, and supplying a low-speed clock signal at the time of appliance control becomes possible at unified type Single Engine.

[0009]Thus, size of a terminal and reduction of power consumption are attained by becoming employable [a clock signal which became employable / IC which unified DSP and CPU /, and was suitable for each of digital signal processing and appliance control].

[0010]As for DSP, it is desirable at the time of a start of appliance control by CPU to receive a command which reduces power consumption from an instruction decoder. By receiving this command, DSP can maintain the state where waiting state (state where operation is suspended although power supply is supplied) electric power is hardly consumed, or can maintain the state where will be in a current supply halt condition and electric power is not consumed. On the other hand, since command decoding for operating DSP to most CPUs and an address arithmetic are made to perform during signal-processing execution by DSP, it does not stop but CPU continues operation.

[0011]When making said CPU perform operation which switches a base station under communication to other base stations, an addition of time may be needed for switch

operation. In such a case, it is desirable to set clock signal frequency at the time of DSP and CPU [both] operation as the 3rd frequency higher than said 1st frequency. A period of both operation becomes brief, therefore a margin of time arises, and said additional time can be secured.

[0012]

[Embodiment of the Invention] Hereafter, the embodiment of the digital communication terminal equipment concerning this invention is described still in detail with reference to some examples shown in the drawing. The same sign used for drawing 1 - drawing 9 shall display the same thing or a prototype.

[0013]

[Example] In <Example 1> drawing 1, the DSP-CPU integrated IC chip in which 301 accommodated DSP and CPU, and 302, The DSP-CPU integrated core which is a body part (a body part is hereafter called "core") of the chip, and 324 show a DSP core, 321 shows a core based CPU, and 313 shows the clock generation circuit in IC chip 301.

[0014] In the figure, 322, 323 each in the core based CPU 321 an instruction decoder, an address generation circuit, and 325, 326, 327, In the DSP core 324, each the register for an operation, a product sum operation machine, an arithmetic operation machine, and 303, Internal ROM (Read Only Memory) 131 and internal SRAM (Static Random Access Memory) 132 in the integrated core 302, The internal bus for delivering and receiving a signal between the DSP core 324 and the core based CPU 321 and 328, The direct connection bus for delivering and receiving a direct signal between DSP core 324 and internal ROM 131 and internal SRAM 132 and 306, The external memory interface for performing signal transfer of external ROM 121 and external SRAM 122 which were installed in the exterior of IC chip 301, and the integrated core 302 via the internal bus 303, The input/output interface in which 311 performs transfer of the audio signal AD/DA (Analog to Digital/ Digital to Analog) converter 106 and digital sound transmission and reception signals (henceforth "SIO"), SIO to which 312 performs transfer of modem AD / DA converter 107, and a digital strange demodulation signal, A peripheral bus for 305 to deliver and receive a signal between the clock signal generating circuit 313, and SIO 311, 312 and the integrated core 302 and 304, The bus control unit for connecting the internal bus 303 to the peripheral bus 305 and 315, 316 show the interrupt signal supplied to the core based CPU 321 from SIO 311, 312, respectively.

[0015] In the figure, 331-334 are connected between clock signal generating circuit 313 and peripheral-bus DS 305, In order to make the clock signal generating circuit 313 generate the internal clock signal 113 of various kinds of frequency in response to

control of the DSP core 321, a digital-signal-processing identification register, a wireless state register, a transmission voice status register, and a received voice status register are shown, respectively. Other composition is the same as that of the conventional terminal. 13 MHz was used for the frequency of the system clock signal 111. The clock signal is for setting up the operation timing of each part of a terminal, stability is required for it, and the temperature control crystal oscillator (TCXO) 101 was used for it as the generation circuit.

[0016]In the above-mentioned composition, at the time of transmission, the audio signal from the microphone 104, After being changed into a digital sound signal by audio signal AD / DA converter 106, in response to digital signal processing (speech compression, grant of an error correcting code, etc.), it becomes a modem DA telephone call sending signal with the DSP-CPU integrated core 302. After the signal receives modem processing with modem AD / DA converter 107, it turns into a radio frequency signal, and power amplification is carried out by the high frequency (henceforth "RF") modulator and demodulator 108 by RF section 109, and it is transmitted from the antenna 110. At the time of reception, the input signal from the antenna 110 turns into an audio signal through this reverse, and is supplied to the loudspeaker 105. The signal which modem AD / DA converter 107 outputs has power monitor data for measuring the radio field intensity from a base station other than a modem AD telephone call input signal at the time of reception. Said digital strange demodulation signal doubles and names generically these and said modem DA telephone call sending signal.

[0017]Next, in DSP-CPU integrated IC chip 301, the instruction decoder 322 decodes the operation command of the DSP core 324, and the operation command of only the core based CPU 321, and, in the case of the operation command of the DSP core 324, gives a control signal at the DSP core 324. The address generation circuit 323 generates the address of internal ROM131 and internal SRAM132. The PLL circuit with a variable multiply ratio was adopted as the clock signal generating circuit 313. the system clock signal 111 supplied to the clock signal generating circuit 313 -- multiplying -- or dividing is carried out, it becomes the internal clock 113, and each [in a chip] block is supplied. Although set up with the registers 331-334, the details are later mentioned for a multiply ratio.

[0018]The digital communication terminal equipment of this example can be used as a terminal used for GSM (Groupe Special Mobile) which is an international-standards system of mobile communications. When the digital communications terminal of this example is in a talk state as a GSM terminal, the CPU-DSP integrated chip 301 performs digital signal processing and appliance control (communications protocol

control and motion control of each part article of the inside of a terminal) by making into a cycle the first-sound voice frame which is 20 ms.

[0019]Digital signal processing is processing which performs conversion with a digital sound signal and a digital strange demodulation signal. As for the transmitting side, a voice encoding process (compression), channel coding processing (error correcting code grant), a modulation process, and a receiver consist of recovery equalization processing, channel decoding processing (digital-error correction), and voice decoding processing (extension). These use arithmetic operation and product sum operation abundantly. The real time nature that the data for one frame must be processed within one frame is required of digital signal processing. For this reason, the core based CPU 321 drives the DSP core 324 at high speed, and realizes digital signal processing. Since programs and data required for digital signal processing are 10 kW (Word) of numbers, and a several kilowatts grade, respectively, they can give the whole quantity to internal ROM131 and internal SRAM132, and performance does not fall victim for external memory access. For this reason, as for the CPU-DSP integrated core 302, in order to realize a required throughput, it is effective to set up the multiply ratio of the clock generation circuit 313 highly in the range which can operate.

[0020]On the other hand, since a program required for appliance control and data amount to 100 kW of numbers, and tens of kW, respectively, they cannot but give most to external ROM121 and external SRAM122. Generally the external memory of low electric power has large access time. For this reason, in appliance control, rate-limiting [of the processing] is carried out with the access speed of external ROM121 or external SRAM122. However, it is effective that external memory sets clock signal frequency below to an accessible value in one cycle in appliance control since real time nature is unnecessary and there are not so many throughputs. Thereby, the excessive power consumption at the time of appliance control is avoidable.

[0021]Since similarly rate-limiting [of the processing] is carried out with the access speed of external SRAM122 also at the time of the settled data transfer processing between external SRAM122 and internal SRAM132, it is effective to set up low clock signal frequency similarly.

[0022]Digital signal processing in the first-sound voice frame (201) which considered these, and the flow of appliance control are shown in drawing 2. The CPU-DSP integrated core 302 first transmits the data which made external SRAM122 memorize, and memorized the modem AD telephone call input-signal data of modem AD / DA converter 107 output for a first-sound voice frame continuously to internal SRAM132 at the time of reception (processing 401). Then, recovery equalization processing (402),

channel decoding processing (403), and voice decoding processing (404) are performed. Once the digital sound input-signal data which digital signal processing ended is saved internal SRAM132, it is sent to audio signal AD / DA converter 106.

[0023]Then, it shifts to processing of transmission, and the CPU-DSP integrated core 302 once stores the digital sound sending-signal data for a first-sound voice frame in internal SRAM132, and a voice encoding process (405), channel coding processing (406), and a modulation process (407) are performed to the stored data. The data after the end of modulation process 407 is modem DA telephone call sending-signal data of modem AD / DA converter 107 input.

Once the data is memorized by internal SRAM132, it is transmitted to external SRAM122 (processing 408), and is sent to modem AD / DA converter 107 after that.

[0024]Next, in order to compare with the power (intensity) of the wave coming from the base station under communication, it shifts to detection of the power of the wave coming from the base station of the circumference of it. The power of the wave coming from the base station under communication is computed by analyzing the amplitude of said input signal. The power of the wave coming from the base station of the circumference of it is detected when the base station of the circumference of it monitors SURROTTO which is communicating with other terminals. For this reason, after the CPU-DSP integrated core 302 makes external SRAM122 memorize the power monitor data for the first-sound voice frame of modem AD / DA converter 107 output, it is transmitted to internal SRAM132 (processing 409). Then, power detection processing (410) is performed using the power monitor data transmitted to internal SRAM132. Then, appliance control (communications protocol control and motion control of each part article of the inside of a terminal) is processed (213). Henceforth, the CPU-DSP integrated core 302 goes into the sleeping 411 from CPU321 in response to a sleep (operation stop) instruction command to the start of the following audio frame.

[0025]The data volume delivered and received by the above transmission and reception is 2500W about a first-sound voice frame. This is a part for the first-sound voice frame of the data of the digital strange demodulation signal delivered and received between modem AD / DA converter 107, and the CPU-DSP integrated core 302, and is data volume produced by giving an over sampling method 4 times which makes four samples correspond to one symbol. The data volume of the digital sound transmission and reception signals delivered and received between audio signal AD / DA converter 106, and the CPU-DSP integrated core 302 is set to 160W about a first-sound voice frame by each of transmission and reception. It is obtained by this performing an 8-kHz sampling

to an audio signal, and one symbol corresponds about one sample.

[0026]Change of the multiply ratio of the internal clock 113 which the clock signal generating circuit 313 generates was doubled and shown in drawing 2. The core based CPU 321 sets the digital-signal-processing identification register 331 as '1' at the time of recovery equalization processing 402 start, and sets it as '0' at the time of the end of modulation process 407. It is again set as '1' at the time of power detection processing 410 start, and is again set as '0' at the time of the end of processing. Thereby, the internal clock signal 113 is set to 52 MHz which multiplied the 13-MHz system clock signal 111 four times during digital-signal-processing execution. On the other hand, each period in appliance control execution, external SRAM transmission processing execution, and sleeping is set to 6.5 MHz which carried out 1 / 2 dividing of the 13-MHz system clock signal 111.

[0027]The core based CPU 321 gives the command of reduce power consumption to the DSP core 324 as a control signal at the time of the end of modulation process 407, and the end of power detection processing 410. The DSP core 324 which received the command operates the clock signal switch (not shown) in the inside, suspends supply of the clock signal to DSP core 324 inside, and goes into a waiting state. In a waiting state, although the power supply is supplied, it suspends operation, and it will be in the low-power-consumption state where electric power is hardly consumed. It is possible to cut off current supply by the command of reduce power consumption besides the supply interruption of the above-mentioned clock signal, and in this case, since there is no current supply, it will be in the state where electric power is not consumed.

[0028]in addition -- transmission and reception come out of the data transfer in IC chip 301, respectively besides having described in drawing 2 -- an 8-kHz periodic interval -- 1 -- the data transfer between audio signal AD / DA converter 106, and internal SRAM132 occurs. [which occurs every / W] Although the frame called a radio frame (26 radio frames are placed every 6 audio frames although mentioned later) is used in the RF modulator and demodulator 108 and RF section 109, 120/26(=4.615)ms which is the cycle have burst transmission of modem AD / DA converter 107 which occurs once [every] each, and the digital strange demodulation signal data between external SRAM122. The sum total of data is set to 625W by the 4 time over sampling method by which the burst transmission makes four samples correspond to one symbol. Burst transmission is started by the interrupt signal 315,316 given to the core based CPU 321 from SIOs 311 and 312. Although the CPU-DSP integrated core 302 suspends operation in the sleeping 411 and only the circumference is operating, if the interrupt signal 315,316 occurs at this time, the CPU-DSP integrated core 302 will be started and the

above-mentioned data transfer will be realized. It goes into sleeping again after ending predetermined processing.

[0029] Said radio frame is a basic motion cycle of RF section 109 and the RF modulator and demodulator 108. 1 radio frame is divided into eight time slots by the time division multiple access (TDMA) method.

To a self-terminal, one of them is assigned to a transmission time slot, and one of further the others [one / other / reception time slot] is assigned to the time slot for power monitors.

The time slot of the remaining others is assigned to another terminal. 26 of a radio frame constitute 1 multiframe for 120 ms, and six of an audio frame synchronize with this. According to the course of modem AD / DA converter 107 ->SIO312 -> external SRAM122, burst transmission of the modem AD telephone call input-signal data is carried out for every end of a reception time slot. Power monitor data also receives the same transmission for every end for power monitors of a time slot. On the other hand, according to the course of external SRAM122 ->SIO312 -> modem AD / DA converter 107, burst transmission of the modem DA telephone call sending-signal data is carried out before a transmission time slot start. The amount of (4x625W) 4 radio frames are [digital strange demodulation signal data] equivalent to a part for a first-sound voice frame (2500W).

[0030] Next, in GSM, operation of the digital communications terminal in the case of performing handover processing which is the processing which switches the base station under communication to another surrounding base station is explained. In advance of explanation, the outline flow of handover processing is shown in drawing 3. In the figure, "MS" is written and "BSS" is written. [a terminal] [a base station] The change to other surrounding base station BSS-B from base station BSS-A while terminal MS is communicating shall be performed.

[0031] First, cover 4 multiframe (501) and the core based CPU 321, a surrounding base station code (BSIC:Base Station Identifier Code) being recognized, then by analyzing the modem AD telephone call input-signal data sent via SIO312 from modem AD / DA converter 107, Electric power is measured and equalized from the power monitor data from each base station, and it aligns at descending (511). Next, electric power and an error rate are measured and equalized from the power monitor data from base station BSS-A (512). Then, these measuring results are put on a control channel, and it transmits to base station BSS-A (513). Base station BSS-A transmits a handover command (Hand Over-command) to terminal MS, when base station BSS-B judges that electric power is the highest from these received measuring results. If the command is

received (514), terminal MS will perform the change to the designated value of synthesizer frequency and a power amplifier output (515). If connection between base station BSS-B and terminal MS is established by this, terminal MS will receive an access complete (Access Complete) signal from base station BSS-B (516). Corresponding to this, terminal MS transmits an access complete AKUNAREJI (Access Complete Ack) signal to base station BSS-A (517), and handover processing ends it.

[0032]The base station change after receiving the above handover command is performed during communication connection, and the processing is performed as appliance control processing. Therefore, the throughput of appliance control increases. When the increment of a throughput cannot be absorbed by the sleeping 411 shown in drawing 2, only the clock signal under digital signal processing is accelerated. It is considered only as the clock signal because processing performance is not improved since rate-limiting [of the processing performance] is carried out at external memory access speed even if it makes quick the clock signal under appliance control processing. In this example, the PLL multiply ratio of the clock signal generating circuit 313 under digital signal processing was raised from 4 times to 9/2.

[0033]Raising of such a multiply ratio foresees generating of a handover, and is performed in the following procedures. When the electric power measurement (511) result from a peripheral base station exceeds the electric power measurement (512) result from the base station under communication and the error rate from the base station under communication exceeds a predetermined value, the core based CPU 321 sets the wireless state register 332 as '1'. At this time, a multiply ratio can be raised to 9/2 near [where the chip 301 can operate] the maximum, and a handover is equipped with it. The core based CPU 321 sets the wireless state register 332 as '0', after handover processing is completed. At this time, a multiply ratio is returned 4 times. Change of the multiply ratio of PLL313 in the first-sound voice frame in the case of being set as the case where the wireless state register 332 is set as '1', and '0' is shown in drawing 4. The processing time of digital signal processing is shortened by clock signal accelerating, and many time of the part appliance control is secured.

[0034]Irrespective of the existence of generating of handover processing, it is also one method to always set the multiply ratio under baseband signal processing as a handover at a correspondence possible value (9/2 twice). However, power consumption is large when the clock signal generating circuit 313 is operated at high speed. Especially, rational number multiplying has many PLL circuit portions which operate compared with integer multiplying, and consumes many electric power. For this reason, as for operating the clock signal generating circuit 31 at high speed, limiting at the time of

handover generating is effective.

[0035]Next, operation of the digital-mobile-communication terminal at the time of detecting a non-sound during a telephone call is explained. In advance of this, the outline flow of the silence detection processing set up in GSM is shown in drawing 5. The silence detection processing in GSM is called VAD (Voice Activity Detection) processing.

[0036]Silence detection processing is performed in the portion of the head of the voice encoding process 405 in the digital signal processing 212. If the DSP core 324 and the core based CPU 321 perform silence detection processing to digital sound sending-signal data and the soundless state of transmission is detected as a result, voice coding of a background noise will be performed and they will transmit the coded background noise as the HO (Hang Over) frame 1111. If a soundless state carries out fourth-sound voice frame part (1101) continuation, the DSP core 324 and the core based CPU 321 will equalize the background noise of this period, and will transmit average value as a SID (Silence Descriptor) frame. Since the DSP core 324 and the core based CPU 321 perform the voice encoding process 405 after storing digital sound sending-signal data as a first-sound voice frame part (160W) voice coding input buffer, The voice encoding process 405 is carried out to the next frame for a fourth-sound voice frame (1101). Since the channel coding 406 and the modulation process 407 have interleave processing, it carries out to the following two frames (1102). The next transmits only a control channel until owner sound detection is carried out again, or until it updates a background noise 480 ms after (1103). Since the voice encoding process 405 turns into only silence detection processing during transmission of a control channel and the channel coding 406 and the modulation process 407 also have only a control channel in an object, the load of processing is reduced substantially.

[0037]A period (1103) until owner sound detection is made by the next or the voice coding of full is resumed for renewal of a background noise, and the transmission voice status register 333 are set to '1' after this period and SID frame formation.

[0038]It is to the SID frame 1121 that a receiver also performs the recovery equalization processing 402 and channel decoding processing 403, and the recovery equalization processing 402 and channel decoding processing 403 are performed only to a period (1131) until it receives an owner sound or the SID frame again, and a control channel after it. The voice decoding processing 404 is interrupted for the next frame of the SID frame (1121), and sending out the fixed background noise of a voice decryption output buffer is continued until it receives an owner sound or the SID frame again after it (1132). For this reason, the load of this period, the recovery equalization processing 402,

the channel decoding processing 403, and the voice decoding processing 404 is reduced substantially.

[0039]After this and after SID frame decoding, an owner sound frame arrives at the next, or the recovery equalization processing 402, and a period (1132) and the received voice status register 334 until it reaches and the channel decoding processing 403 is resumed of full are set to '1' for renewal of a background noise.

[0040]The processing-load mitigation at the time of the above silence detection was made to reflect in the clock-signal-frequency fall under digital signal processing, and reduce power consumption of the clock signal generating circuit 313 was performed. Change of the multiply ratio in a first-sound voice frame in case the transmission voice status register 333 is set in 'the received voice status register 334'1 when set to 1" is shown in drawing 6. Respectively, reduction of the transmitting side and a receiver throughput is utilized, and the multiply ratio under digital signal processing is reduced by 3 times from 4 times.

[0041]In this example, although aimed at the audio signal, this invention can be applied to other signals, such as not only this but a video signal, and a FAX signal, and the same effect can be acquired.

[0042]In <Example 2> digital-signal-processing period 212 (refer to drawing 4), the digital communication terminal equipment made to correspond when it was required that an internal clock signal should be accelerated even in the range for which fixed rational number multiplying is not of use is shown in drawing 7. In the figure, the oscillator which generates the clock signal in which 701 is asynchronous as for the system clock signal 111, and 702 show the input-clock change register which switches the signal inputted into the clock signal generating circuit 313 to the system clock signal 111 or an asynchronous clock signal. The change register 702 performs switch operation in response to control of the core based CPU 321.

[0043]As described above, the frequency of the 9/2 twice as many internal clock signal which carried out rational number multiplication as this is 58.5 MHz about a 13-MHz system clock signal. On the other hand, when the CPU-DSP integrated chip 301 can operate to 60 MHz, it is effective to obtain still higher frequency, but. If it is going to obtain it by rational number multiplying, it will be set to 59.71875 MHz by 73/16 time as many rational number multiplying by 59.3125 MHz and 147/32 time as many rational number multiplying. However, if such complicated multiplying is made to perform to a PLL circuit, circuit structure and power consumption will increase increasingly.

[0044]For this reason, a 13.33-MHz clock signal with the 13-MHz asynchronous system

clock signal 111 is used, it is multiplied $9/2$, and 60 MHz was obtained. However, since the clock signal which does not synchronize mutually will be used within radio equipment, the harmonics of an asynchronous clock signal or the product ingredient of the system clock signal 111 and an asynchronous clock signal may arise as an interference in a transmitting and receiving band. In that case, the period of the transmission time slot 802 of the TDMA system shown in drawing 8, the reception time slot 803, and the time slot 804 for power monitors is avoided, and an asynchronous clock signal is used. Control to the change register 702 is performed when the core based CPU 321 writes '1' or '0' in the change register 702. In the case of '1', the system clock signal 111 is chosen, and when it is '0', an asynchronous clock signal is chosen.

[0045]

[Effect of the Invention]In this invention, regular use of the high speed clock signal which heightens power consumption is avoided by becoming employable [the clock frequency which became employable / the IC chip which unified DSP and CPU /, and was suitable for each of digital signal processing and appliance control].

Therefore, the size of a terminal and reduction of power consumption are attained.

Since it becomes employable [the clock frequency which was suitable for each at the time of silent of the change of a base station, and a sound], much more reduce power consumption of a terminal becomes possible.

[Translation done.]